Sensors & Actuators: B. Chemical 331 (2021) 129323

Contents lists available at ScienceDirect

Sensors and Actuators: B. Chemical

journal homepage: www.elsevier.com/locate/snb

Optimized electrochemical breakdown etching using temporal voltage variation for formation of nanopores in a silicon membrane

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ARTICLE INFO

Keywords:
Nanopore
Electrochemical breakdown etching
High-aspect-ratio
Silicon membranes

ABSTRACT

Dielectric breakdown etching is a well-known method of making nanopores on thin (~50 nm) dielectric membranes. However, voltage driven translocation of biomolecules through such nanopores becomes extremely fast. For improved detection, for instance by the current blockage, a high-aspect-ratio nanopore could be beneficial for slowing down the translocation. High-aspect-ratio nanopore on silicon fabrication requires a well-controlled process and is dependent on specific crystal orientation, dopant type and resistivity of substrate. Therefore, an optimized method of processing high-aspect-ratio nanopores is necessary considering the advantage of a silicon membrane being able to be integrated with standard CMOS processing. Here, we present an optimized fabrication method for mass-producing a single and an array of nanopores on a thick (2 μm) silicon device layer based on a silicon-on-insulator (SOI) wafer. A method of temporal voltage variation is exploited to optimize the etching parameters for the nanopore formation during electrochemical breakdown etching, diameters of nanopores around 12 nm have been achieved. Besides, the correlation between the parameters of etching and nanopore diameter is deduced. The processed high-aspect-ratio nanopore enables applications in single-molecule sensing such as DNA, exosomes, viruses, and protein markers. The developed process is inexpensive, fast and can be batch fabricated.

1. Introduction

Nanopores, in particular, solid-state nanopores with a diameter scale of 10 nm have gained considerable interest for their applications in various fields such as human genome sequencing, ion filtration with high selective character [1,2], nanoparticle detection [3–6], hemofiltration [7], protein sensing [8], and virus detection [9]. These nanopores are fabricated from various materials. Different diameter scales of nanopores are obtained by using different materials such as Al_2O_3 [10,11], graphene [12], silicon nitride [13–15], MoS_2 [16], HfO_2 [17] and silicon [18]. Another type of nanopore, called "biological pores", is derived from proteins, such as MspA [19,20], and α-hemolysin [21]. In comparison between solid-state nanopores and biological nanopores, the solid-state nanopores show higher signal-to noise ratio when using a high sampling rate to record the signal [22–24]. Therefore, solid-state nanopores are found more stable at higher voltages and bandwidths. Among solid-state nanopores, the ones based on silicon offer many advantages due to its compatibility to be integrated into the standard silicon CMOS technology [25]. Mass-fabrication of silicon nanopore chips may therefore revolutionize single-molecule sensing-based research and clinical applications with high throughput and low-cost sensing devices. With nanopores on a silicon substrate, the detection of DNA translocation can be improved due to a sharper spike of current blockage [26]. To obtain a large array of nanopores with desired pore sizes for various target molecules, a variety of nanopore fabrication methods on silicon have been reported recently: Anisotropic KOH etching on pre-patterned silicon membranes by e-beam lithography were used to produce nanopores of diameters in the range of 10–100 nm [27–30]. Ling et al. used high laser power to fabricate pores with a large diameter scale, around 200 μm [28]. Nanopores on a thin silicon nitride (SiN) with a diameter of approx. 2 nm has been processed using controlled dielectric breakdown etching [31–33]. Nanopores have been processed in several other materials including silicon nitride membranes by a combination of e-beam lithography and reactive ion etching [34].

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https://doi.org/10.1016/j.snb.2020.129323
Received 30 July 2020; Received in revised form 28 October 2020; Accepted 2 December 2020
Available online 29 December 2020

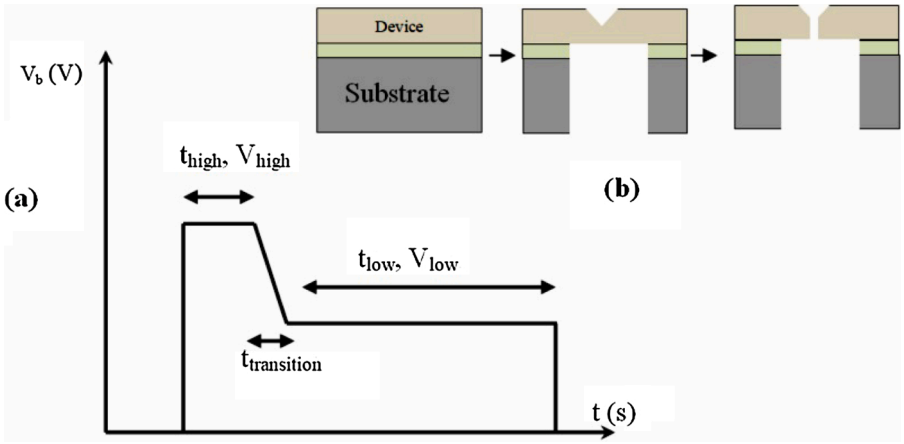

Fig. 1. Schematic of the voltage model to produce nanopores and nanopore formation in an SOI wafer. (a) Schematic of the voltage-time model with high voltage, transition and low bias regions for electrochemical breakdown etching to achieve a nanopore. (b) Schematic depicting UV lithography on SOI wafer to produce templates of the inverted pyramid structure. The templates are used for producing nanopores using the electrochemical breakdown etching.

However, e-beam lithography-based methods are relatively expensive and time-consuming. Anisotropic KOH etching suffers from large pore size variation inherited from the variation in membrane thickness and the lithography step. Furthermore, several methods are identified to slow down the translocation time of biomolecules such as piranha cleaning and atomic layer deposition of ZnO [35,36]]. Recently, our group has shown that a high-aspect-ratio nanopore can be used with a longer DNA translocation time [37].

To address the above-mentioned problems as well as to improve the aspect ratio of nanopore, we have earlier demonstrated a mass-fabrication of high-aspect-ratio nanopores in silicon by electrochemical etching with illumination [38]. Arrays of nanopores of diameters ranging from 8 nm to 100 nm with aspect ratio over 10 were fabricated. However, low reproducibility of pore sizes between batches due to the lack of breakdown process control hinders the further applications of this method. Although, an alternative approach of using illumination to generate electron-hole pairs to sustain electrochemical reaction was reported to decouple pore etching from the applied voltage in bulk silicon substrate [38]. Using illumination on a thin membrane often results in uncontrollable large pore size due to excessive amount of electron-hole pairs in the confined space [39]. Therefore, a nanopore etching method with a controllable pore size in a broad range and high reproducibility is still challenging.

In this work, we present a novel electrochemical etching method to fabricate nanopores on silicon membranes by using temporal voltage variation (time optimized multi-step-voltage model) to control the breakdown etching. This method is an illumination-free method and the electron-hole pairs in the silicon created by the avalanche effect under high voltage. This results in a high-aspect-ratio nanopore with high reproducibility. The novelty lies in the method of in-situ modulation of voltage and time duration according to the pore geometry to obtain a high-aspect- ratio and small nanopore diameter. This method is repeatable and the diameter of the nanopore correlates to the voltage model and the duration of etching. Using this method, we obtain nanopores with length of approx. 1000 nm and with a diameter below 10 nm. This method allows for a standardized processing method, which lowers the cost of production. The silicon chips containing the nanopores are processed in the clean room. Hence, inherently the yield is high. Moreover, the fast processing of nanopores using electrochemical breakdown etching and low cost method of processing has advantages in batch processing of silicon chips. The silicon nanopores can be processed in wafer-level and hence has the potential to scale-up. The processed-high-aspect-ratio nanopore is suitable for a wide range of applications in biomolecule sensing such as DNA, exosomes, viruses, and protein markers. With this process, we could envision high throughput fabrication of nanopores (single as well as arrays) with accurate diameters.

2. Materials and methods

In this section, we present a detailed analysis of electrochemical breakdown etching. The novel part in this method is the variation of the applied electric voltage to control the geometry of the growing pore. This allows the user to have significant control over the process of producing high-aspect-ratio nanopores.

2.1. The description of nanopore formation process

During the process of electrochemical etching, the dissolution of silicon occurs under anodic potentials when immersed in an HF solution. Positive charged carriers or holes (h^+) in silicon are generated by an electric breakdown in this reaction. Avalanche breakdown dominates in the moderately (or low) doped silicon, the free carriers in the space charge region (SCR) are accelerated by the high electric field and collide with crystal lattice thereby freeing the bound electrons. In this situation, the current density (J) is limited by the mass transport of the electrolyte [40]. Therefore, when J is less than a critical current density (which depends on the HF concentration, absolute temperature and the activation energy), the divalent reaction occurs [41]:

$$Si + 2F^- + 2h^+ \rightarrow SiF_2 \quad (1)$$

$$SiF_2 + 2HF \rightarrow SiF_4 + H_2 \quad (2)$$

where, h^+ represents the holes in silicon. On the pyramid-structured silicon surface, the field strength increases with the decreasing radius of structure curvature, lowering the required voltage to trigger an electric breakdown. Thus, the breakdown can begin selectively at the pore tip. As the pore etching progresses, the radius of the pore tip decreases. As a result, a voltage lower than the initial one is needed to maintain breakdown etching selectively at the sharpest tip, which enables a minimized pore diameter. Each chip is etched by the voltage model in Fig. 1(a).

The voltage model is selected based on the experimental results of several iterations of electrochemical breakdown etching. Two constant voltage values corresponding to two regions of voltage named as high-bias (V_H) and low-bias (V_L) regions are applied. V_H is used to initiate nanopores at the tip of inverted pyramids on the front side by creating a tip with a high curvature. However, from the previous report, for etching using backside illumination [18], high voltage coupled with illumination can generate an unexpectedly large amount of positive charges on

Table 1
Temporal voltage variation for investigating the best bias profile to obtain narrow nanopores on a silicon device layer in an SOI wafer.

Region	High bias	Transition	Low bias
V_b (V)	13.5–18.0 V	Linearly variable	7.0 V
t(s)	13–14 s	20	Variable

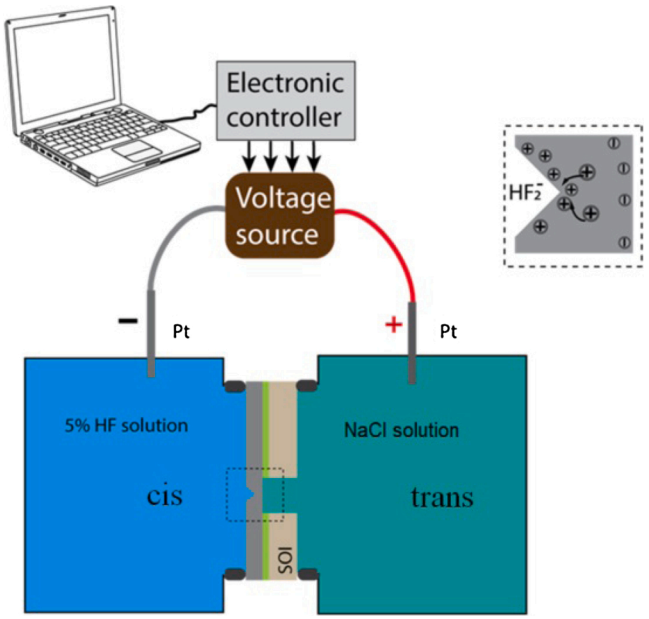

Fig. 2. Schematic of the etching setup. The SOI chip containing the template for nanopore formation is placed in between the two chambers. One of the chambers is filled with 5 %HF solution and the other is filled with NaCl and ethanol solution. The voltage is varied using an external circuit that is controlled by a Matlab program. The inset schematic shows the reaction occurring at the tip of the inverted pyramid structure.

the wall of the nanopores leading to uneven electric field distribution making the walls rough. Therefore, the electric field distribution around the tip of the inverted pyramid is carefully controlled to have a uniform electric field distribution during etching. The following variation of voltage (V_b) – time (t) as shown in Table 1, is observed to find optimal bias profile. Between high and low bias regions, durations of 20 s for transition region (t_{trans}) is fixed, and the voltage value of the low bias region is fixed at 7.0 V for all experiments. A schematic of processing a high-aspect-ratio nanopore in the device layer of the silicon chip produced by UV lithography and KOH etching, then etched by electrochemical-breakdown method from the device layer is shown in Fig. 1(b).

2.2. Electrochemical etching setup

The silicon on insulator chip containing the template for producing a nanopore is placed in between the two chambers. One of the chambers is filled with 5 %HF solution and the other is filled with NaCl and ethanol solution. Two platinum electrodes which are inert to aggressive electrolyte are connected to the two chambers and a voltage is applied between them. A power supply is connected to an external electronic circuit consisting of controller using a home-built MATLAB® program.

The processed chip is mounted on a home-built PTFE cell that is filled with 5 % HF: H_2O: C_2H_5OH (1:8:3) solution on the device side of the chip (cis) and NaCl solution (9 mg/ml) on the handle layer of the chip (trans) as shown in Fig. 2. Two O-rings are contacted the both sides of the chip to avoid any leakage. When V_b is applied between the two electrodes in the electrochemical cell, the bottom tip of the inverted pyramid experiences a stronger field strength due to high curvature and thin membrane thickness. This effect allows the electric field strength to reach the threshold of breakdown (3×10^5 V/cm) at the bottom tip of the inverted pyramid as compared to a planar surface. In addition, the anisotropy of the etching, rate plays an important role in the formation of straight pores. The current density is the highest along (0 0 1) direction of the silicon crystal thus the pores tend to grow along the (0 0 1) direction since the current density equals to the critical current density due to the assumption that a tetravalent reaction occurs [41,42].

Inverted pyramid template processing: A series of chips with inverted pyramid templates are processed on 15 mm × 15 mm sized chips of an SOI wafer. A 4-inch-silicon wafer with 3 layers: device layer, n-type (2 ± 0.5 µm) with a resistance of 1–5 Ω.cm^{-1}, buried oxide(BOX) layer (1 µm) and handle silicon layer (500 ± 25 µm). A square opening with a size of 2 µm × 2 µm is created using UV lithography on the device layer. The inverted pyramid is formed using 30 %wt KOH for a total duration of 200 s at 80 °C. For the electrolyte contact with the device layer, a large square opening of the size 100 µm × 100 µm is etched by using DRIE from the back of the silicon substrate. The results of the ICP etching are checked by using an optical microscope to ensure that the residual silicon layer on the backside of the device is completely etched.

2.3. Nanopore fabricated by electrochemical breakdown etching

After fabricating the front and the back sides of membranes, chips are cleaned by two types of RCA-cleaning solutions. The RCA-1 contains the mixture of NH_4OH, H_2O_2 and deionized water with a volume ratio of 0.2:0.2:1.0 to remove organic residuals on the surface of membranes. Next, chips are soaked inside a solution consisted of HCl, H_2O_2 and deionized water, the volume ratio of this mixture is 0.2:0.2:1.0 for metallic contamination cleaning (RCA-2). The cleaning processes are conducted at 80 °C for 5 min. The electrochemical-breakdown-etching setup used to process nanopores is shown in Fig. 2. To control voltage and record current during etching, a homemade circuit with relays is operated by a Matlab script. All the etching processes are carried out at room temperature.

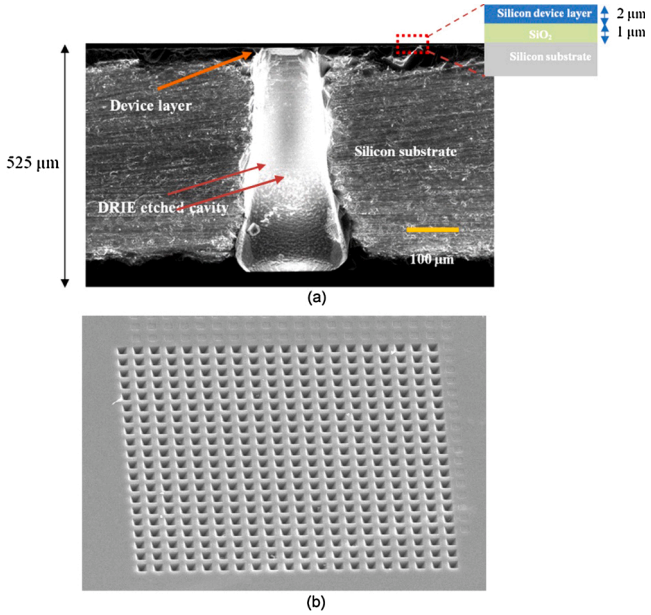

Fig. 3. Cross-sectional images of the nanopore and SOI chip, (a) Cross-section-EM image of an SOI wafer showing the deep-reactive-ion etched region of silicon substrate wafer that allows suspending a 2 µm thick device layer. (b) SEM image of the device layer showing an array of 20 × 20 inverted pyramids with a nanopore on each inverted pyramid processed by KOH etching and electrochemical breakdown etching.

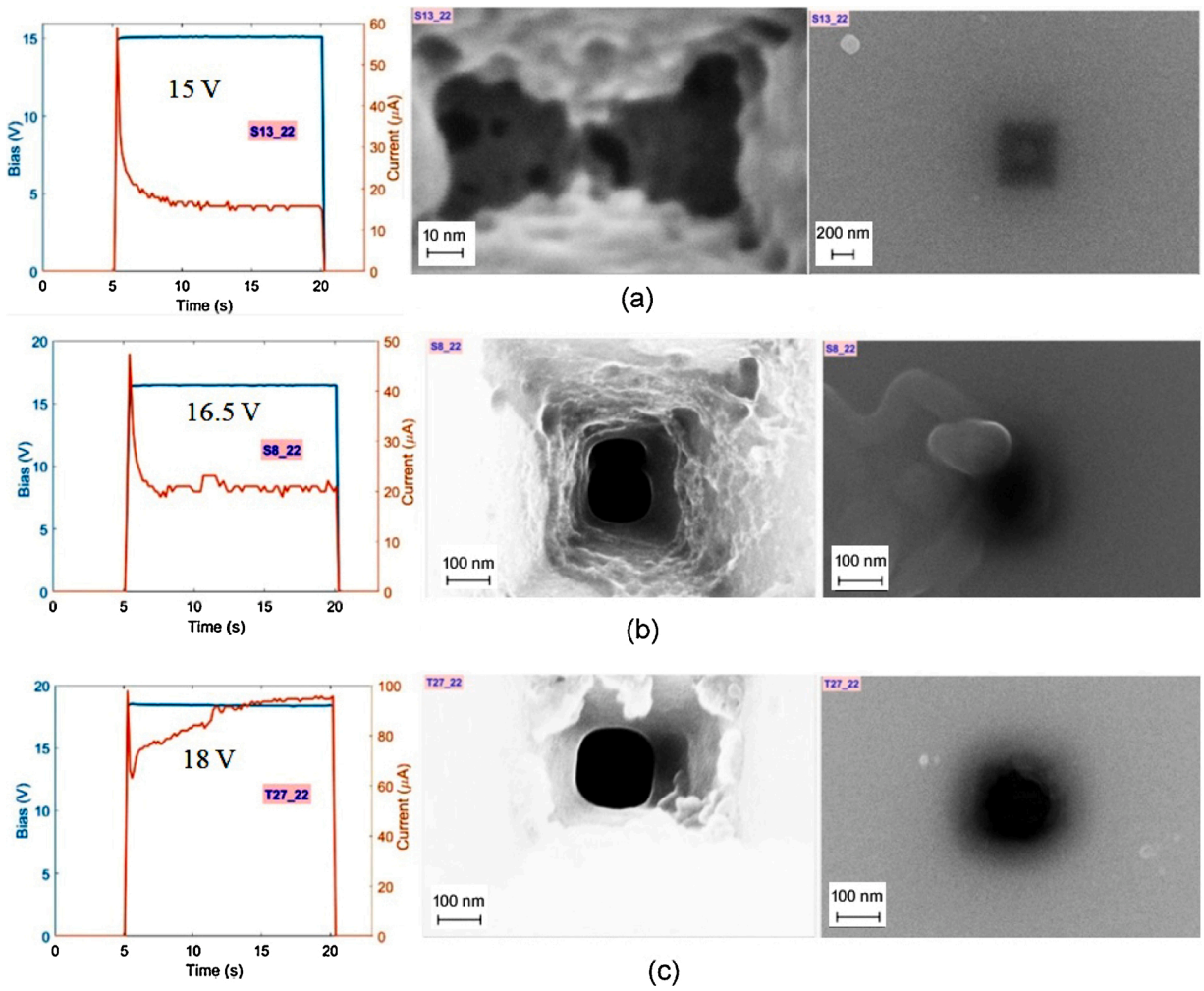

Fig. 4. A combination of images shows the results achieved during high voltage etching at several single voltages. In each panel (horizontal), left: voltage model (blue), current trace (red), middle: SEM image of nanopore on front side and right: SEM image of backside of etched chips. Panel (a): results of model of 15.0 V for 14 s on S13_22 chip. The SEM image of the frontside shows about 30–40 nm wide nanopore. Panel (b): chips S8_22 show clearer nanopore formation as etched by a bias of 16.5 V. Panel (c): chip T27_22 shows a very clear large nanopore as the result of 18.0 V bias. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

2.4. Conductance measurements and DNA translocation experiment

In order to investigate the potential of these etched nanopores for DNA translocation, the chips at first are cleaned by piranha solution (H_2SO_4:H_2O_2 = 3:1) followed by RCA-1 at 80 °C for 5 min and RCA-2 at 80 °C for 5 min cleaning. Finally these nanopores are processed by oxygen plasma for 2 min for surface treatment. We believe that these steps increases the wetting of nanopores. After the cleaning steps, the conductance measurements are performed with KCl solutions of different concentrations and pH values as shown in Fig. 10(b) and 10 (d). In the next step, an experiment to investigate DNA translocation through the nanopore in terms of current blockage is carried out. Both conductance and DNA translocation experiments use a fast amplifier (40 kHz sampling rate) PICO 2 to generate bias and record current.

3. Results and discussion

The following section describes the electrochemical breakdown etching from twelve SOI wafers with 26 devices on each of them. Each chip is processed by the voltage-time model in Fig. 1(a). The modulation of voltage-time and its effect on the nanopore diameter are investigated. The roles of high bias, transition and low bias regions are investigated in detail and their effects on electrochemical breakdown etching will be discussed.

The SEM image in Fig. 3(a) shows the cross-section of the SOI chip. A large-deep-reactive-ion-etched (DRIE) cavity is used for electrolyte filling that connects the nanopore on the device layer. The silicon substrate allows suspending a 2 μm thick device layer that houses the nanopores. Fig. 3(b) shows the KOH etched template with nanopores distributed in an array on the device layer. To examine the cross-section profile and the length of the nanopore, the chip is cut and imaged using a focused ion beam (30KV, FEI Nova 200 dual beam system).

3.1. The role of high bias region

To investigate the role of the high bias region, a rectangular voltage pulse is applied between the two electrodes. In this method, three voltage values, namely 15.0, 16.5 and 18.0 V are applied for etching three identical chips then they are investigated for nanopore formation by SEM. The experimental results are showed in Fig. 4. This section presents the role of low bias region on the nanopore formation by modulating its duration as the high bias region is fixed. The setup remained the same as in Fig. 2. As can be seen in Fig. 4, three identical samples are etched in the single high bias region. The chip S13_22 is etched with a voltage of 15.0 V for 14 s. The SEM images from the front side and back side of the device layer indicate the initiation of a large

Table 2
The effect of high voltage on the diameter of nanopores.

V_b (V)	Duration t (s)	d_{pore} from the backside of the device layer (nm)
15.0	14	No pore
16.5	14	50–70
18.0	14	100–150

nanopore in the range of 30–40 nm as can be seen in Fig. 4(a). However, there is no clear evidence of nanopore formation on the back side of the membrane. Two remaining chips are etched in the same condition as the first chip with a higher voltage, namely 16.5 and 18.0 V. As can be seen from Fig. 4(b), a 100 nm wide nanopore is etched from the top side. The back-side image shows that a nanopore starts to appear with a size in the range 50–70 nm. The results of the sample T27_22 etched by 18 V for 14 s is shown in Fig. 4c. From the current trace, it can be noted that the ionic current increases over time indicating an enlargement in the diameter of the nanopore. It could be possible to estimate the enlargement rate from the pore during etching. From the SEM images, we can observe that the diameter of nanopore on front side and back side are 170 nm and 100 nm, respectively. From the above results, we can see that breakdown etching starts at the tip of the inverted pyramid at 15.0 V. However, a large nanopore diameter is observed. Further tuning of the voltage may be necessary to achieve a small-diameter nanopore.

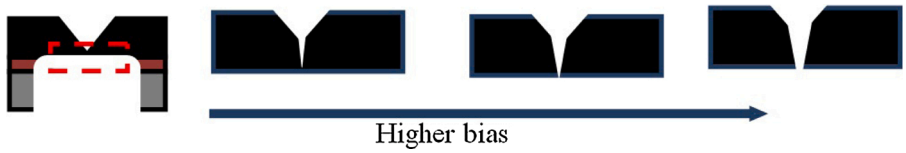

Fig. 5. A schematic diagram of the tip of the inverted pyramid as the bias is increased in the high bias region.

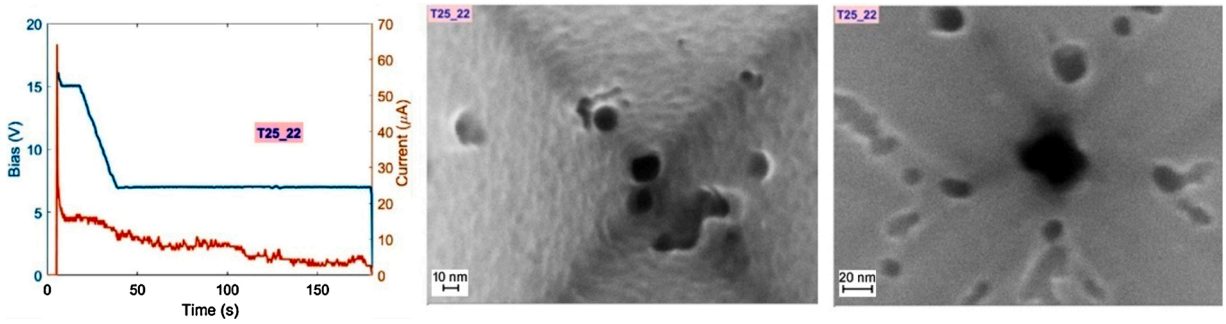

Fig. 6. The applied voltage model and the SEM images of nanopores on chip T25_22. A combination of high and low voltage models to achieve a long and narrow-high-aspect-ratio nanopore with a duration of 142 s.

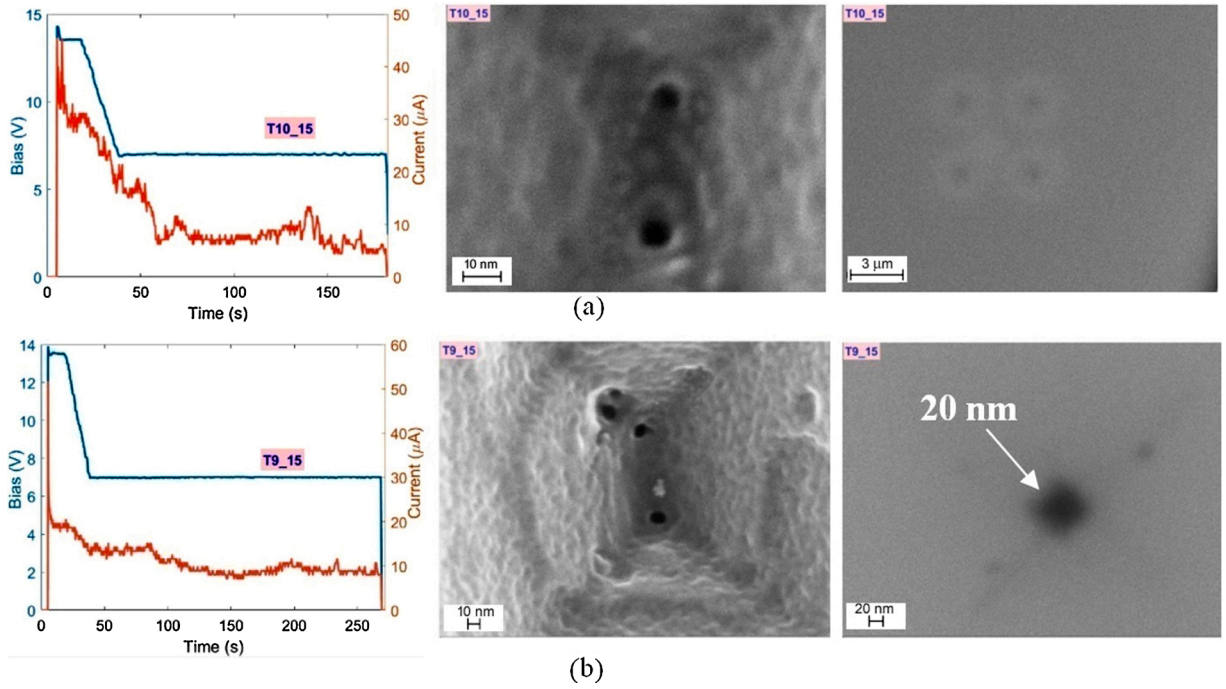

Fig. 7. Optimized etching model with high, transition and low bias regions. (a) SEM images of chip T10_15 etched by voltage model with a short low bias region (left), the images of the front side (middle) and backside (right).(b)The optimal parameters for both high and low bias region to get small nanopore applied for chip T9_15. Here a high bias region is set by 13.5 V and 14 s, while the low bias region relates to 7.0 V and 230 s.

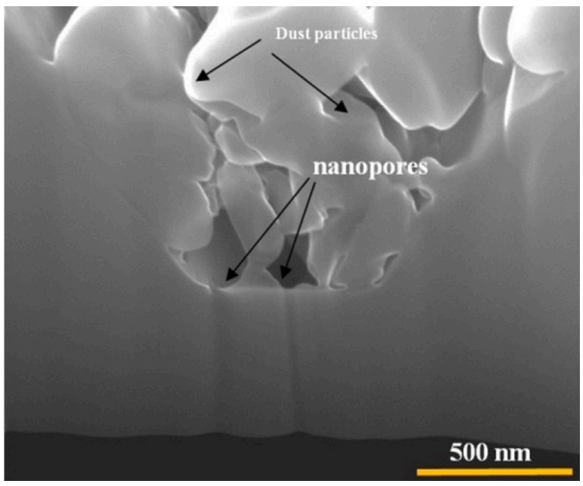

Fig. 8. The SEM image of a cross-section of another etched nanopore using FIB on the T9_15 chip showing the straight and high -aspect-ratio nanopores with a diameter of 20 nm.

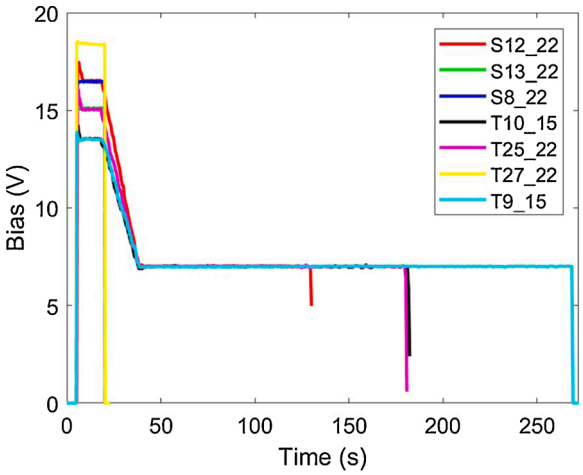

Fig. 9. Etching voltage model after optimization of the etching process for seven devices. Configuration of voltage to the etching time, with the diameter of the nanopore showing various nanopore diameters.

Therefore, it can be concluded that the value of voltage and duration of high bias region are important parameters that affect on the overall radius of the nanopore at the end of the etching. A smaller initial diameter that can be achieved with high voltage could lead to a smaller diameter of nanopore at the exit. Hence, a voltage of 15.0 V or lower could be an optimum starting point for a smaller diameter nanopore to initiate at the tip of the inverted pyramid. This is an important value that would determine the further voltage-temporal model of the electrochemical breakdown etching.

The effect of high voltage on the diameter of the nanopore is reported in Table 2. An explanation of the advancement of the etching model during high voltage is schematically depicted in Fig. 5. It is observed that of the tip of the inverted pyramid enlarges as the bias is increased in the high bias region. The nanopore takes a "conical" shape with a large diameter at the entrance and a smaller diameter at the exit. When a voltage of 15.0 V for 14 s is applied, it is observed that a small pore initiates on the front side. As the voltage is increased to 16.5 and 18.0 V in the same condition, the nanopore becomes larger. The proof for pore formation on the backside is clearer for a higher voltage. As we predict, a higher voltage results in a higher growth rate of a nanopore in the direction (0 0 1) and makes nanopore larger. Therefore, in order to obtain a smooth and straight profile of the nanopore, there is a need for a combination of a high bias and a low bias since a single model of high bias is not sufficient to create a cylindrical, straight and high-aspect -ratio nanopore.

3.2. The role of low bias region

Following a high voltage model with a voltage of 15.0 V for 14 s and a 20s-transition region, a low-bias region with a voltage of 7.0 V is fixed and a variable duration is investigated.

The effect of a long low-bias region is shown in Fig. 6 where the applied voltage model and the SEM images of nanopores on chip T25_22 are displayed. A combination of a high and a low voltage models to achieve a high-aspect-ratio nanopore with a duration of 142 s becomes apparent. The front side and back side of pore are approx. 15 nm and approx. 25 nm, respectively, indicating an outward conical structure of the nanopore. Therefore, the low voltage appears to continue "drilling" the nanopore on the direction (0 0 1) much faster than on other directions.

3.3. Optimized and predictive etching parameters

To etch a high-aspect-ratio nanopore with a cylindrical, straight, and narrow wall, there is a need for an optimized voltage temporal model for the electrochemical breakdown etching. In this section, optimized and predictive etching by the combination of high and low voltage model is described. As can be seen in Figs. 4 and 6, the diameter of the nanopore on the frontside mainly depends on the high bias region (both duration and voltage value), while that on the backside relates to the low bias region (also both duration and voltage value). The smaller diameter relates to a lower voltage and shorter duration. However, if the duration is too short, the nanopore is not completely etched. Therefore, an optimum value of etching parameter is needed. As shown in Fig. 7a, under low voltage duration of 144 s, the small nanopore (around 8 nm) is seen, but there is no proof of nanopore formation on the backside (low magnification). However, if the low voltage is maintained up to 230 s, as shown in Fig. 7b, the nanopore on the frontside is almost similar to that in the previous figure, but there is clear evidence for the existence of a nanopore on the backside of the membrane with a diameter around 20 nm. Fig. 8 shows an SEM image of the cross-section of a single inverted pyramid obtained from FIB etching. The image shows the cross-section of the device layer with a straight profile of the nanopores with a diameter of 25 nm. The etching of the device using KOH resulted in an inverted pyramid with a depth of 1.4 μm and the length of the nanopore is approx. 600 nm.

Seven chips from different batches of wafers are etched and their bias profiles are plotted in Fig. 9 , their diameter values are listed in Table 3.

The variation of the high bias region and the transition region is from 13.5 to 18.0 V and the transition time is 0 s or 20 s. The steady-state time is from 0 s to 230 s. The diameter variation with the optimized etching is small with clear proof of nanopore on both back and front sides. For our SOI wafer, the optimal high bias region is found to be 13.5 V for 13 s and followed by a low voltage of 7.0 V with a duration of 230 s. It should also be noted that the optimization model is subjected to several parameters such as the doping concentration, temperature, orientation of the wafer, the resistivity etc. Therefore, a careful estimate is necessary to reproduce the results reliably and effectively.

The temporal-voltage model for optimization of the electrochemical breakdown etching to produce narrow, cylindrical nanopores could help in applications for biosensing, physical nanopore arrays etc., and could replace a more common conical nanopore [43].

In the batch of samples, a nanopore with a diameter around 15 nm is selected to measure the conductance. The conductance measurements is performed on the nanopore using KCl buffer with the concentration of 0.1 M under 3 different pH values, i.e., 5.5, 7.3 and 8.6, the results are shown in Fig. 10(a). The current-bias relation is showed in Fig. 10(a) for 3 different pHs, while variations of conductance for different pH values

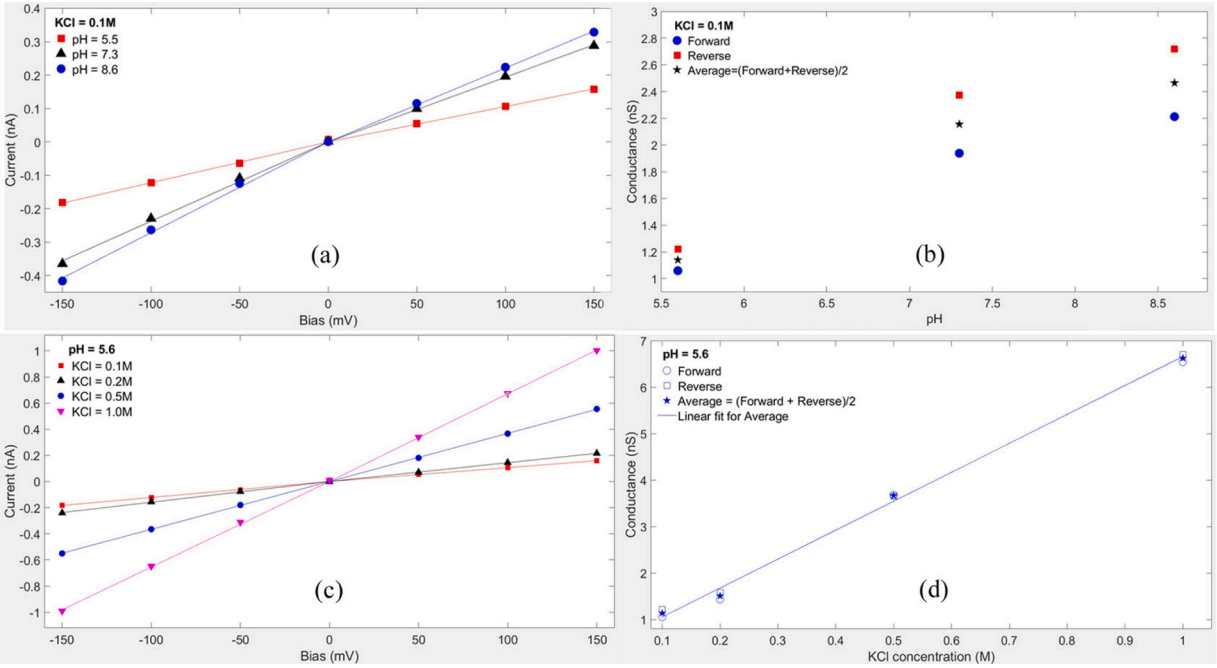

Fig. 10. (a) The relation between current and bias for KCl concentration of 0.1 M for 3 pH values, namely 5.5, 7.3 and 8.6. (b) The conductance at different pHs are deduced from the linear fittings of the dataset from panel (a). (c) The ionic current at various KCl concentrations with a constant pH of 5.6. It is seen that as the concentration increases the conductance increases. (d) The linear relation between the KCl concentration and the conductance.

Table 3
The detailed study of voltage, and the relation to the diameter of the nanopore.

No	Chip	V_H (V)	t_H (s)	t_{trans} (s)	V_L (V)	t_L (s)	d_{front} (nm)	d_{back} (nm)
1	S13_22	15.0	14	0	0	0	30–40	–
2	S8_22	16.5	14	0	0	0	100	50–70
3	T27_22	18.0	14	0	0	0	170	100
4	S12_22	15.0	13	20	7	92	20	10
5	T25_22	15.0	13	20	7	142	15	30
6	T9_15	13.5	13	20	7	230	12	20
7	T10_15	13.5	13	20	7	144	8	Blur

are shown in Fig. 10(b). The conductance increases for higher pH concentrations but the dependence is not linear. The rectification effect is found by using linear fitting functions for 2 regimes, namely positive (forward) and negative (reverse) biases. We observe an increase in nanopore conductance with increasing pH, as shown in Fig. 10(b). This can be attributed to the increased osmotic flow induced current due to increased negative surface charge at high pH [44].

The conductance of a nanopore with a diameter of 15 nm under different KCl concentrations is investigated. For a pH of 5.6, four KCl concentrations, namely 0.1, 0.2, 0.5 and 1.0 M are used. The characteristic of the nanopore at different KCl concentrations is shown in Fig. 10(c) and 10 (d). The variation of ionic current to bias at different

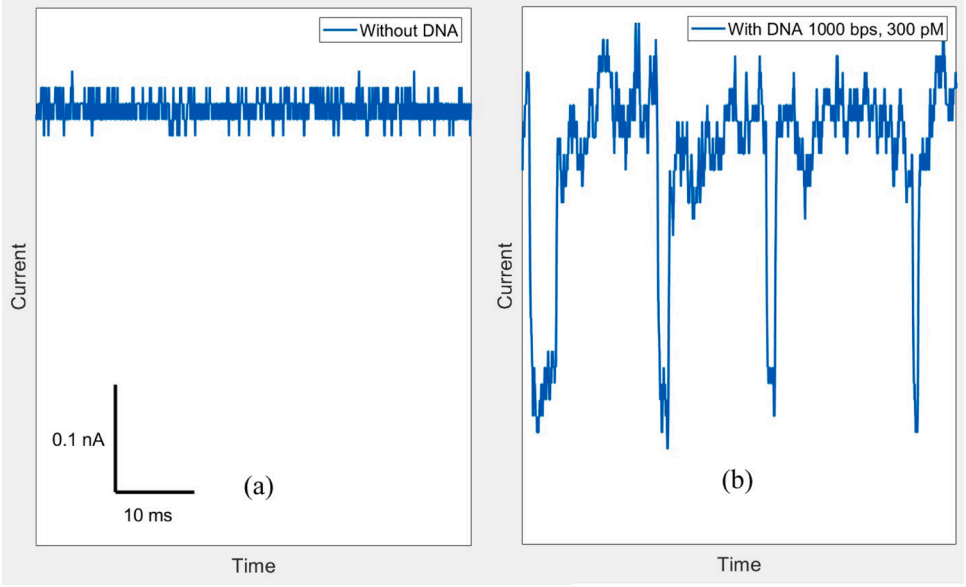

Fig. 11. The ionic current of the nanopore with and without DNA. (a) the ionic current across the nanopore when a voltage of 600 mV is applied. (b) When ds DNA of 1000 bps is inserted into the cis chamber of the chip. The amplitude is measured to be approx. 250 pA and the duration of event is approx. 1 ms.

KCl concentrations is shown in Fig. 10(c) and the variation of conductance with KCl concentration is shown in Fig. 10(d). The nanopore conductance increases with the concentration of KCl, indicating the detected current is indeed the ionic current through the nanopore.

We performed biosensing experiments to verify nanopore for DNA translocation. A single nanopore with diameter of approx. 15 nm is selected, KCl 1.0 M solution is used as a solvent to dilute DNA strands (300 pM with 1000 bps) under a bias of 600 mV. Fig. 11(a) shows the ionic current trace when 1.0 M KCl buffer is used, while Fig. 11(b) shows current blockage duration around few ms with an amplitude of around 250 pA. Because of this translocation rate, the amplifier with moderate bandwidth can be used for single molecule detection using these nanopores. This allows for a several applications of the nanopores such as protein sensing, exosome detection and virus translocation detection. However, the big challenge of this nanopore is its enlargement under high bias and high laser illumination, so the bias amplitude and illumination dose must be considered when molecule translocation through nanopores is investigated.

4. Conclusion

In summary, we present for the first time a novel method of optimized electrochemical breakdown etching for producing nanopores in a silicon substrate with high aspect ratio using temporal voltage variation. The method presented in this report is low-cost, fast and requires minimum control parameters. The optimal profile of bias allows to fabricate nanopore with diameter down to 10 nm. The wafer level processing method allows for several chips to be fabricated at once allowing for a low-cost chips. In addition, formation of nanopores using electrochemical etching is fast (approx. 20 min). Both single and array of nanopores can be processes with this method. The correlation between bias profile and diameter of nanopore is found and can be used to make desired nanopores. The voltage model with two bias regions results in clear nanopore formation, the relation between voltage model (both voltage value and duration) and diameter of the nanopore is clearly seen: longer duration and higher voltage leads to larger nanopores. The model could be useful for producing cylindrical, high-aspect-ratio nanopores. In future, we plan to integrate a feedback control system that would allow the formation of nanopores using the temporal voltage control method. This would allow us to process many nanopores in a repeatable and reliable way within a short duration of time.

Authors' contribution

Nguyen Xuan Chung: System installation, experiment, data process, writing, submission and revision. Hithesh Kumar Gatty: System installation, experiment, data process, writing and revision. Xi Lu: Experiment and revision. Miao Zhang: System Installation and revision. Jan Linnros: Supervision, revision and funding.

Declaration of Competing Interest

The authors report no declarations of interest.

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